



REPLACEMENT SHEETS

Title: METHOD FOR TESTING FOR THE PRESENCE OF FAULTS IN DIGITAL CIRCUITS

Inventor: Richard Illman - Serial No. 09/808,325

Docket No. CAF-27202/03

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```
SCAN_TEST =  
    pattern = 0;  
    apply "grpl_load" 0 =  
        chain "chain_0" =  
"11111101011100001111100011100110110101000001010010\  
10001100000111000110100001101001110010001010011110\  
11011100011000010001100011110010001001010100000011\  
10101010010011001011011001011001100100000110010010\  
01110100000000111101111011001100111010111011010010\  
00100111111001010110100001001100000011000011101101\  
10101111011011010001101100111001000110100011011100\  
10101111100100000001110110010000110011000011111000\  
0001001000101011001110111000111111111100111100111\  
01011000111001111101000110001111011101110011100111\  
00100011010101100101010111000101010101111010011000\  
00110111110111011101111001110100010010001000011111\  
1110110001001110110111100111011111011011100110011\  
11110111000110000101111100001000011100111111101111\  
01010000100000010001101010101111101001110110110100\  
01111011111011111111101001101011001110001100010100\  
1101111011110010000100001011111111110000010110011\  
10010011001110011110101000000110100101001100011010\  
1110000010101101011010100101101111111010011110001\  
00011010011111101100010100110110101011010100100110\  
10111110101011100010000100111000011000011000010111\  
01101101100000110011010011000011011000001011110110\  
11010011011110000110001001110001110110101001000110\  
1100000110111111111101111011010010001101010000011\  
1011011001000101100001100010011110101011111011001\  
11110001010001000110001110011101011100001000100000\  
10110110111010010011001001110110010010100010110111\  
10011100101100110110010011000001010110101011110100\  
01010000101101101100100101011000010011011100010110\  
00111110001010111110000000100101000011011000001100\  
0001110111001000011100100000101100000101100011100001";
```

Prior Art

Fig. 1(a)

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```

chain "chain_1" =
"10111100101010100011111100111000110110011011001111\
0111001110100110011111011000011101010101011110110\
00111010001000110110101011010101010010010000100101\
01001010100001101001100100110110000010011000001010\
01010011100000000101010110110000111111010001010001\
01011000101011110011101100100110011110100011011000\
00111111100000011101100000001110011111011001100110\
11011100000000001000101011100001111110001101000110\
11011001000000011000111010001011101110011010101111\
0001000101011011001001111111011001000001111110000\
11100100011101110011011001011011000110111011001100\
00110001100010110111101001011101011100001011010010\
00011011010100111101001001011010100111011000110101\
01010000001100110100000011111100100101000001100011\
00000111010111011000010100011100011001110100010101\
0100001000000000011011110001001001100101000000111\
01010001110101000001000100000011000011000001010101\
1010001101101111000000110000011011001001110111110\
01001000101101000101110110111101000000111010000010\
10001101111100100001110101110110101101000011101110\
10110000101000110100111101100100100011110100011111\
0010101111100000011101110111101010001101000100011\
00010011001110110100001101110000101001110111110110\
11000001100101110110101101010011110101101000001111\
01001111011000111111100001001110001100110001011000\
10101110101101010100000010100010111111101110111011\
10001110010010100100001101001101100011001011110101\
010000100000000111101000111101100010010000000101001\
11111110100110001011011110101000001010001110000001\
1100101000110110010010110110110001101111110011010\
0111110001111111000001001100011011101100000";

```

Prior Art

Fig. 1(b)

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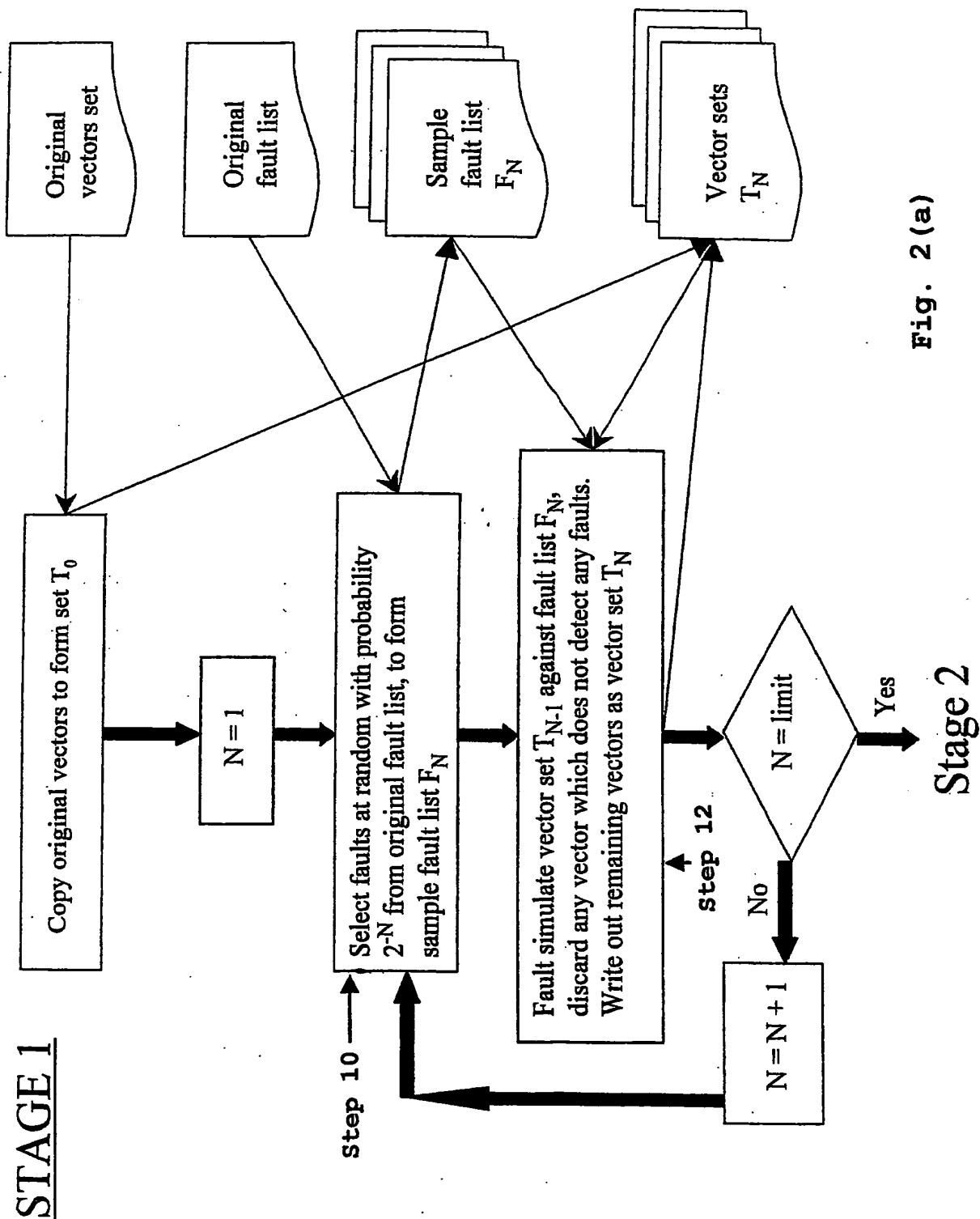


Fig. 2(a)

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STAGE 2

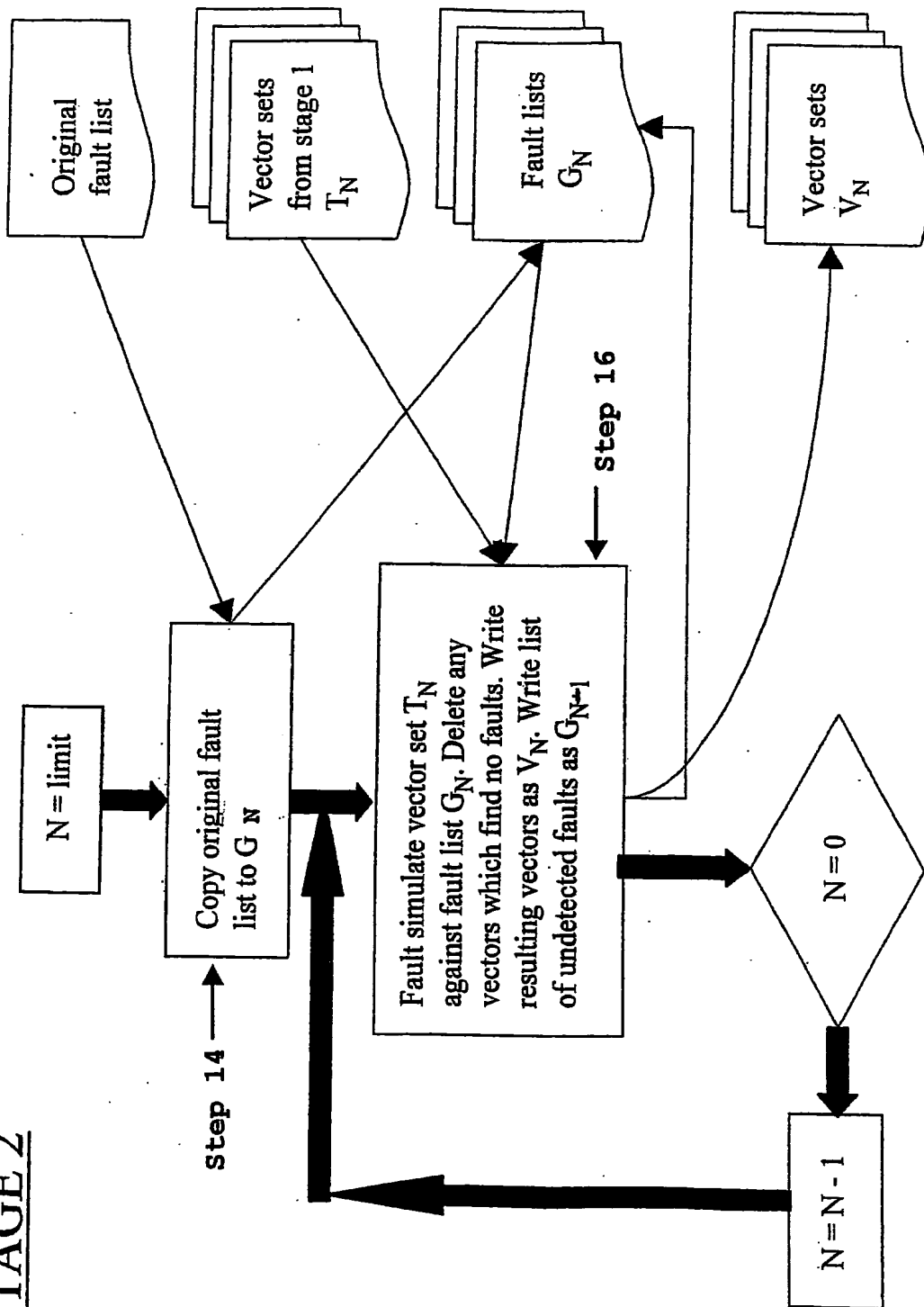


Fig. 2 (b)

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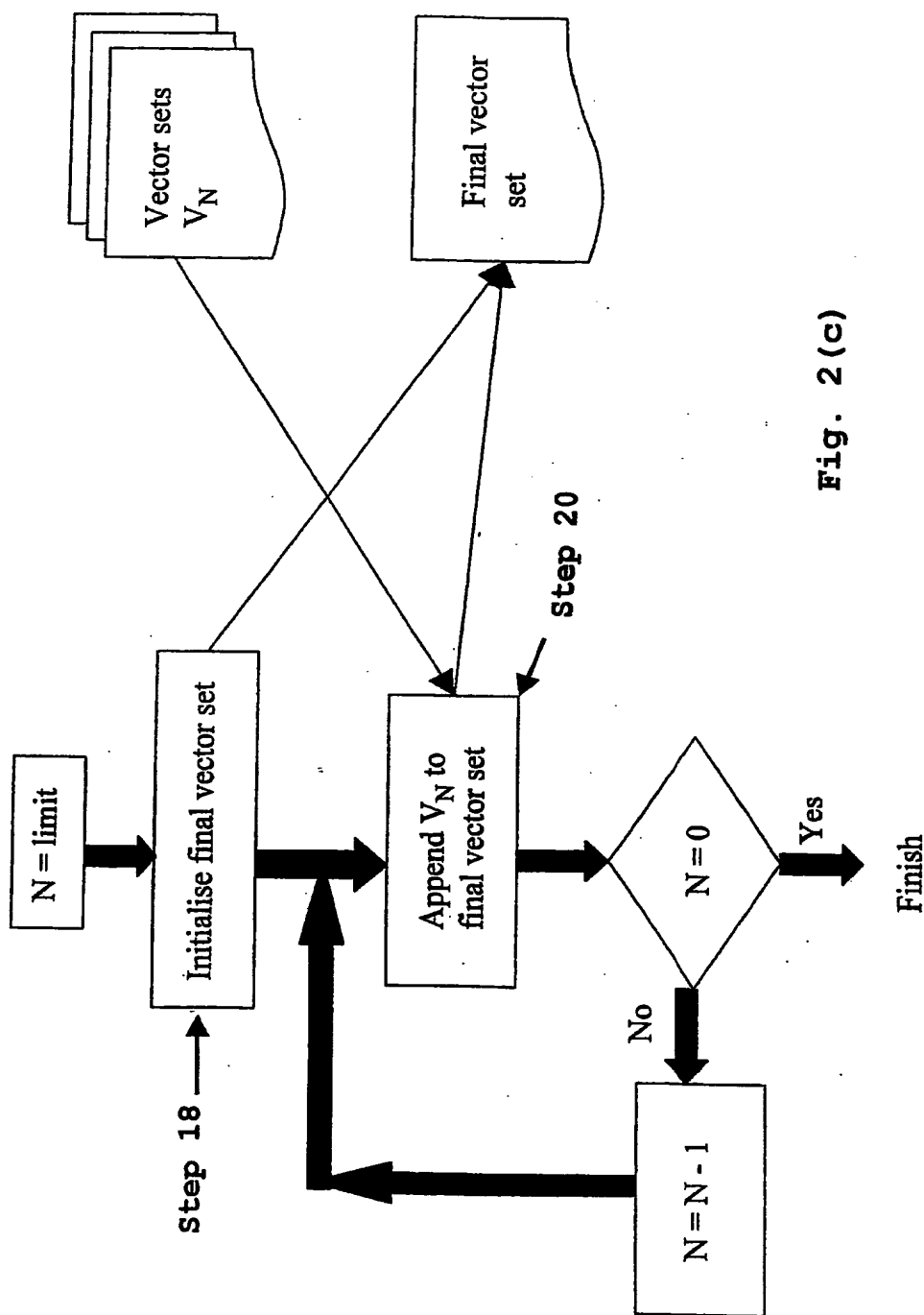


Fig. 2(c)

STAGE 3

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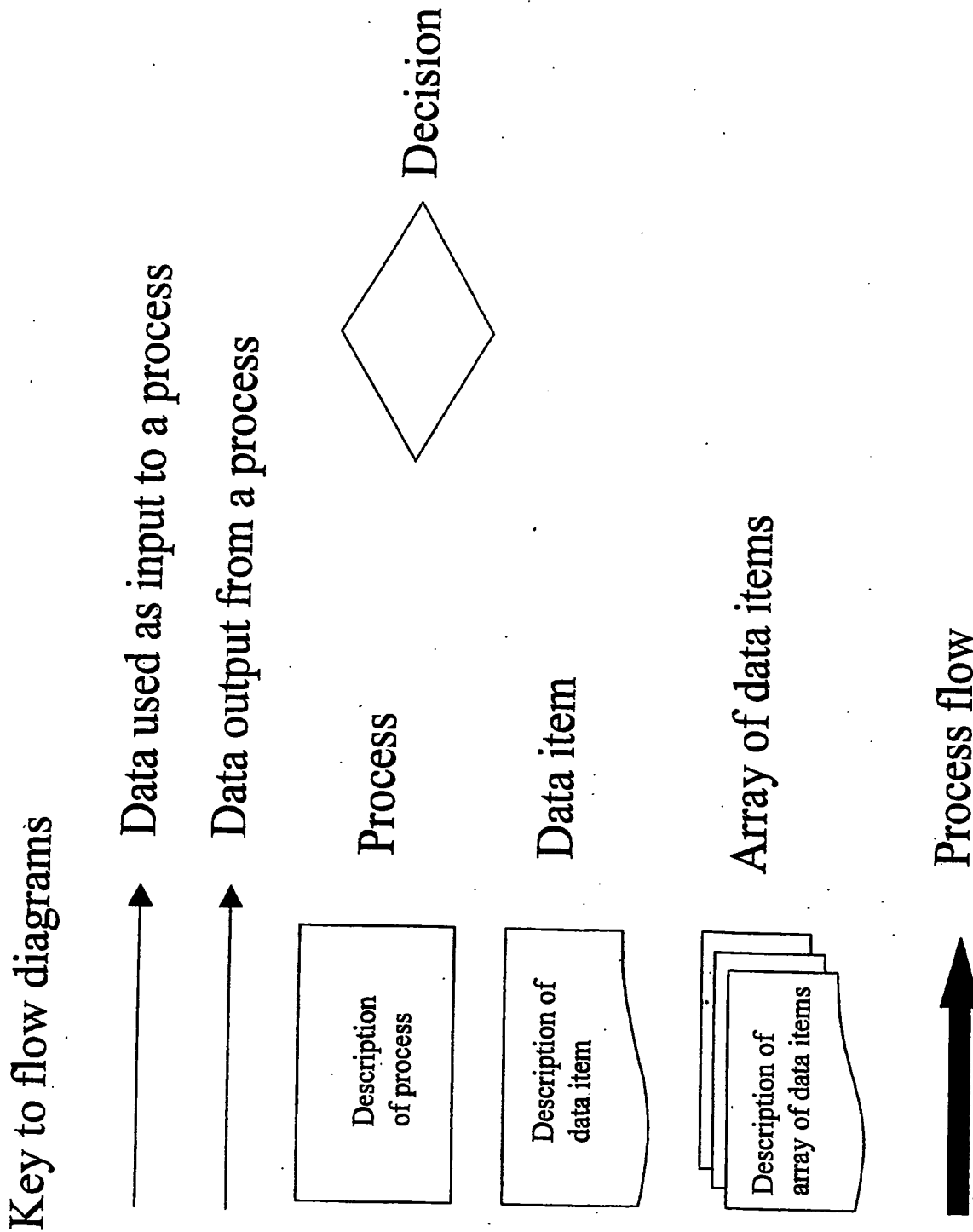


Fig. 3

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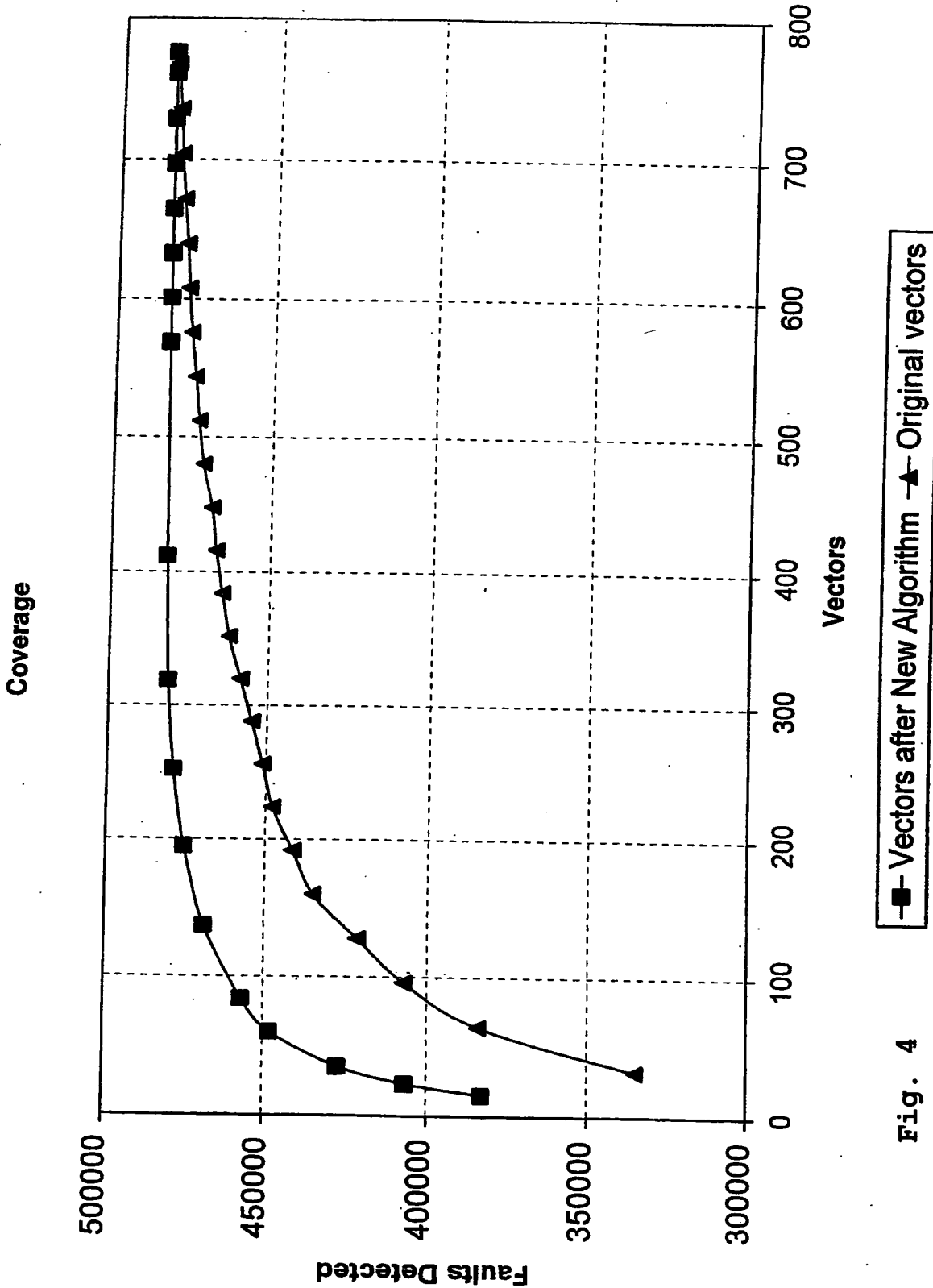


Fig. 4